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**AMENDMENTS TO THE DRAWINGS:**

The attached sheet of drawings includes changes to Fig. 1. This sheet replaces the original sheet containing Fig. 1. In Fig. 1, applicant has added the legend --Prior Art--.

Attachment:      Replacement Sheet

REMARKS

The office action of May 17, 2005, has been carefully considered.

It is noted that the drawings are objected to on various grounds.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) over the patent to Tanigawa et al.

Claims 8-9 are rejected under 35 U.S.C. 103(a) over Tanigawa et al. in view of the patent to Kameshima.

Finally, claims 3-7 would be allowable if rewritten in independent form.

In connection with the Examiner's objections to the drawings, applicant has amended claim 1 to include the legend --Prior Art--, and has amended claim 1 to delete the optical detector module, the meter, the rotary member and the reflective sector. With these changes it is respectfully submitted that the objections to the drawings are overcome and should be withdrawn.

In view of the Examiner's rejections of the claims, applicant has canceled claim 2 and amended claim 1.

It is respectfully submitted that the claims presently on file differ essentially and in an unobvious, highly advantageous manner from the constructions disclosed in the references.

Turning now to the references and particularly to the patent to Tanigawa et al., it can be seen that this patent discloses a light projecting circuit in a photoelectric switch. In Tanigawa et al., the LED 23 is connected to the circuit composed of the transistor 21 and the resistors 22, 24, 25. This circuit is a constant current generator. The amplitude of the current pulse generated in the LED 23 is constant and independent of the supply voltage  $V_c$ .

In the presently claimed invention, on the other hand, the capacitor  $C_e$  is preloaded through the bias resistor  $R_{pol}$  which results in a current pulse being proportional to the supply voltage. This is not disclosed by the reference.

Furthermore, Tanigawa et al. use the charging circuit

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composed of resistor 91 and capacitor 92 for increasing the supply voltage of the driving circuit 2 momentarily during the generation of the current pulse. This is necessary when the supply voltage  $V_c$  has an insufficient value for compensating the voltage decreases in the driving circuit 2 (voltage decrease in LED 23 added to the voltage decrease in the circuit composed of resistors 22, 24, 25 and transistor 21). In contrast, the resistor  $R_{pol}$  and the capacitor  $C_e$  of the presently claimed invention are used to generate a current pulse proportional to the supply voltage. This is not disclosed by Tanigawa et al.

In view of these considerations it is respectfully submitted that the rejection of claims 1 and 2 under 35 U.S.C. 102(b) over the above-discussed reference is overcome and should be withdrawn.

The patent application of Kameshima discloses a photoelectric conversion apparatus having a controllable power supply 4 that generates a voltage  $V_{s1}$  or  $V_{s2}$  that is applied to photodiodes P1 to P4. The electric charges resulting from illumination of the photodiodes are stored in storage capacitors C1 to C4. A gate drive unit 3 emits a gate pulse  $V_{g1}$  or  $V_{g2}$  for control of on/off transistors T1 to T4, allowing a reading unit 2 to read the charges stored in the storage capacitors. A comparator 5 connected

to the reading unit compares the respective charges stored in C1 to C4 with a threshold voltage Va.

In column 4, lines 37-40, Kameshima states that "the reading unit is composed of amplifiers, an analog multiplexer, an A-D converter, a memory, etc...not illustrated. This reading unit 2 is normally composed of external IC or the like." The capacitors C1 to C4 are connected, through the transistors T1 to T4, to the reading unit which is a complex device as indicated above. The non-inverted input of the comparator is not directly connected to the anode of the photodiodes, but through a transistor and the reading unit 2.

The Examiner combined Tanigawa et al. with Kameshima in determining that claims 8 and 9 would be unpatentable over such a combination. Applicant respectfully submits that the combination of references does not teach the invention recited in independent claim 1 presently on file.

In view of these considerations it is respectfully submitted that the rejection of claims 8 and 9 under 35 U.S.C. 103(a) over a combination of the above-discussed references is overcome and should be withdrawn.



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Reconsideration and allowance of the present application are respectfully requested.

Any additional fees or charges required at this time in connection with this application may be charged to Patent and Trademark Office Deposit Account No. 19-2825.

Respectfully submitted,

By

  
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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450 Alexandria, VA 22313-1450, on August 15, 2005.

By:

  
Joseph Sofer

Date: August 15, 2005